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REMARKS

Prior to this Response, a final Office Action was mailed January 3, 2003.

In the Office Action, claims 5-7 and 9 were rejected.

In this Response, claim 5 is amended. No new subject matter is added.

The amendment to claim 5 constitutes a bona fide attempt by the applicant to advance the prosecution of the application and obtain allowance. It is believed that the amendment to claim 5 places claims 6, 7, and 9 in condition for allowance as well.

Claims 5-7 and 9 remain pending in the present application. Reconsideration is respectfully requested in light of the following remarks.

Claim Rejections – 35 USC § 103

Claims 5-7 and 9 stand rejected under 35 U.S.C 103(a) as being unpatentable over Subramanian et al. (US Patent No. 5,668,021) in view of Applicant Admitted Prior Art (AAPA). Claim 5 is amended. It is believed the amendment to claim 5 places it in condition for allowance.

Claim 5 now recites that the first surface region of the impurity implantation region comprises the longest part of the impurity implantation region. This distinguishes it from the egg-shaped region 24 shown in Subramanian FIGS. 2-7.

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CONCLUSION

The Subramanian reference and the AAPA do not teach or suggest all the claim limitations of claim 5.

Accordingly, applicant submits that claim 5 is patentable over the combination of Subramanian and the AAPA. Likewise, it follows that dependent claims 6-7 and 9 also are patentable, at least for the reason of being dependent upon a patentable base claim.

In view of the above, applicant submits that claims 5-7 and 9 of the present application are allowable and respectfully request such action for this case.

The Examiner is encouraged to telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,
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I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Box AF, Assistant Commissioner for Patents, Washington D.C. 20231 on: _____

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

5. (Amended Four Times) A pull-up transistor disposed between a Vdd terminal and an I/O pad of a semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a source region and a drain region of a second conductivity type formed in the substrate and defining between them a channel region, one of the source region and the drain region being electrically coupled to the I/O pad, the other one of the source region and the drain region being electrically coupled to the Vdd terminal;

an impurity implantation region of impurities of a second conductivity type formed in a first sector of the channel region, the first sector not reaching either one of the source region and the drain region;

the impurity implantation region [of the first sector] comprising a first surface region of the second conductivity type [as a depletion channel] on the semiconductor substrate, wherein the first surface region comprises the longest part of the impurity implantation region;

a second sector of the channel region exclusive of the first sector comprising a second surface region of the first conductivity type on the semiconductor substrate with uniform doping concentration [of the first conductivity type and a surface region of the first conductivity type as an enhancement channel];

a gate insulating layer on the substrate over at least a portion of the first surface region [of the first sector] and the second surface region [of the second sector]; and

a gate on the gate insulating layer over at least a portion of the first sector and over at least a portion of the second sector.